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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,019	12/10/2003	Sang Ik Jung	SI-0052	5195

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EXAMINER	
KRAVETS, LEONID	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,019	JUNG ET AL.	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-11 and 20-23* is/are rejected.

7)☒ Claim(s) *4,7 and 12-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of the foreign priority papers filed December 10, 2003 claiming priority from Korean application 10-2002-0083582 filed on December 24, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-6, 8-11, 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli (US Pub No 2003/0009631.

4. As per claim 1, Arimilli discloses a cache flush system, comprising:

a valid array unit configured to provide cache block information for an update algorithm and index information for a cache flush algorithm of at least one cache block in a prescribed state (Paragraph 95);

a storage unit configured to store tags and provide match address information for the update algorithm and tag information for the cache flush algorithm (Paragraph 56);

a bus snooper configured to perform the update algorithm for the tag storage unit and the valid array unit by monitoring a processor bus and by tracing a state of each cache memory (Paragraph 68); and

a cache flush unit configured to detect a system event, to perform the cache flush algorithm for corresponding cache blocks in the prescribed state (Paragraph 90).

5. As per claim 2, Arimilli discloses the system of claim 1, wherein the storage unit comprises:

a tag RAM unit configured to store a plurality of tags for a prescribed index (Paragraph 56); and

a match logic unit coupled to the tag RAM unit configured to provide whether processor bus address matches a tag of corresponding address index by outputting the match address information, and wherein the match logic unit is configured to provide a tag that will make up address for a read transaction by outputting the tag information (Paragraph 56).

6. As per claim 3, Arimilli discloses the system of claim 1, wherein the bus snooper performs the update algorithm by operating placement algorithm using cache block information from a prescribed logic operation [All computer operations are logic operations, thus the snooper of Arimilli uses a prescribed logic operation to perform the update algorithm (Paragraph 68-69)].

7. As per claim 5, Arimilli discloses the system of claim 1, wherein the cache flush unit comprises:

an event detector configured to detect whether the system event occurs (Paragraph 93);

a cache flusher configured to generate a read transaction for a corresponding cache block according to the index information and the tag information to which a corresponding address is mapped, by performing the cache flush algorithm (Paragraph 94); and

a cache bus master configured to perform the cache flush algorithm for the cache memory by transferring the read transaction to each processor through outputting the generated read transaction to the processor bus (Paragraph 93).

8. As per claim 6, Arimilli discloses the system of claim 5, wherein the cache flusher extracts a corresponding index by performing an address arrangement using index information from a prescribed logic operation, obtains the tag information from a match logic unit
of the storage unit providing the index and maps the address by incorporating the index and the tag (Paragraph 58).

9. As per claim 8, Arimilli discloses the system of claim 1, wherein the prescribed state is a valid state including a modified state and an exclusive state, and wherein the cache flush unit generates a read transaction to perform the cache flush algorithm for

the cache block in the valid state and outputs the read transaction to the processor bus [The system of Arimilli uses MESI protocol (Paragraph 82), which includes the modified, exclusive and valid states (Paragraph 95).

10. As per claim 9, Arimilli discloses a cache flush method, comprising:

updating status information by monitoring a transaction of a processor bus and tracing states of cache memory corresponding to each processor (Paragraph 94); and

flushing at least one cache block in a prescribed state among the cache blocks by detecting a prescribed event, generating a read transaction using the status information and outputting the generated read transaction (Paragraph 94).

11. As per claim 10, the method of claim 9, wherein said updating status information comprises:

determining whether an attribute of the transaction is read by monitoring start of the transaction on the processor bus and by extracting an attribute of the transaction (Fig 5);

determining whether a share attribute is asserted from a processor except for a transaction master processor for the read attribute of the transaction, and wherein when the share attribute is asserted from the processor when a processor whose address matches the share assertion exists, clearing a corresponding valid bit of the address matched processor to set an invalid state and not setting a corresponding valid bit of the transaction master processor as a valid state (Paragraph 79-80).

12. As per claim 11, the method of claim 10, wherein said updating status information comprises:

receiving cache block information using a placement process in a case where the share attribute is not asserted (Paragraph 81); and

storing tags in a location, designated by an index corresponding to the address in a certain cache block, according to the cache block information and setting a valid bit of the corresponding cache block as the valid state (Paragraph 81 and 84).

13. As per claim 20, Arimilli discloses the method of claim 9, wherein the prescribed state is a valid state, and wherein the status information includes tag information and a valid status information (Paragraph 94).

14. As per claim 21, Arimilli discloses a multi processor system, comprising:

a plurality of processors coupled to a processor bus (Fig 2a, Ref 58, 60);

at least one cache memory coupled to each processor (Fig 2a, Ref 62);

a memory controller coupled to the processor bus (Fig 4, Ref 156);

and a cache flush system coupled to the processor bus, wherein the cache flush system comprises (Paragraph 90),

a first unit configured to provide cache status information (Paragraph 44);

a second unit coupled to the first unit and configured to update the cache status information (Paragraph 68); and

a third unit coupled to the first unit and configured to detect system events to perform cache flushing for corresponding cache blocks in a prescribed state responsive to the detected event (Paragraph 90).

15. As per claim 22, Arimilli discloses the system of claim 21, wherein the second unit is configured to update the cache status information by monitoring the processor bus and by tracing a

state of each cache memory (Paragraph 68).

16. As per claim 23, Arimilli discloses the system of claim 21, wherein the first unit comprises:

a valid array unit configured to provide cache block information for an update algorithm and index information for a cache flush algorithm of at least one cache block in a prescribed state (Paragraph 95);

a tag storage unit configured to store tags and provide match address information for the update algorithm and tag information for the cache flush algorithm (Paragraph 56).

Allowable Subject Matter

17. Claims 4, 7 and 12-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

18. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is (571)272-2706. The examiner can normally be reached on Mon-Fri 8-430.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonid Kravets
Patent Examiner
Art Unit 2189

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER